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REMARKS

The specification has been amended to correct typographical errors.

The Abstract has been amended as suggested by the examiner to overcome the objection.

Claim 19 has been amended as suggested by the examiner to overcome the objection and not to overcome a rejection based on a statutory requirement.

Applicants acknowledge with appreciation the notice of allowable subject matter of Claims 2, 4-10, 12 and 14-20, however, Applicants submit that these claims are distinguishable over the prior art of record for reasons not limited to those presented by the examiner, and that the record speaks for itself.

Claims 1-20 are pending in the application.

Applicants respectfully request reconsideration and examination of Claims 1-20 in view of the amendments above and the arguments below.

By way of this response, Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain any outstanding issues that require adverse action, it is respectfully requested that the examiner telephone Timothy R. Croll at (408)433-7625 so that such issues may be resolved as expeditiously as possible.

Response to the rejection under 35 U.S.C. § 103

Claims 1, 3, 11 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Vo, et al., U.S. Patent Application Pub. 2005/0022085 A1 (Vo). Applicants traverse the rejection as follows.

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Claim 1 recites steps of generating a navigation map of test paths for an integrated circuit die, selecting a grid spacing to define a grid map of cell locations from the navigation map for each of the test paths, and calculating a value for each of the cell locations that is representative of the difference between a total number of the test paths intersecting each of the cell locations and a failed number of the test paths intersecting each of the cell locations.

Regarding Claims 1 and 11, the rejection alleges that Vo teaches selecting the claimed grid spacing to define a grid map of cell locations from the navigation map for each of the test paths in paragraphs [0022]-[0034]. However, Vo does not mention the claimed grid spacing or the claimed selection of a grid spacing. Further, the selection of a grid spacing is not relevant to Vo's method. As Vo teaches in paragraph [0033], the SFI tool identifies resources that occur most frequently in the failed test paths. Vo does not teach or suggest defining a grid map of cell locations that are intersected by test paths as recited in Claims 1 and 11.

The rejection further alleges that it would be obvious to include the claimed calculated value for each cell location in Vo because the claimed calculated value would likely be used in Vo to define a greater probability of defining a defect in an integrated circuit. Because Vo lacks the claimed cell locations defined by the claimed grid spacing, however, there is no basis in Vo for calculating the claimed calculated value for each cell location. Further, Vo is not directed to finding a probability of a defect. As Vo teaches in paragraph [0037], Vo identifies failed resources, not a probability that the resources are defective. Because Vo is not directed to finding a probability of a defect, the motivation does not exist in Vo for calculating the claimed

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calculated value for each cell location as alleged by the rejection.

Because there is no motivation in Vo to calculate the claimed value for each of the claimed cell locations, and because Vo lacks the claimed grid spacing selected to define the claimed cell locations, and because Vo does not teach or suggest defining a grid map of cell locations that are intersected by test paths, the modification proposed by the rejection fails to arrive at the claimed invention, therefore Claims 1 and 11 are not obvious under 35 U.S.C. § 103(a).

Regarding Claims 3 and 13, the rejection alleges that it would be obvious to select a grid spacing of 50 to 200 microns to provide sufficient channel for routing test paths. However, the rejection does not explain why a grid spacing of 50 to 200 microns would be obvious over any other grid spacing that provided sufficient channel for routing test paths. The criteria for selecting the claimed grid spacing of 50 to 200 microns are defined in the paragraph beginning on page 6, line 24 of the specification as follows:

"The selected grid spacing 302 defines the size of the cell locations 306. The size of the cell locations 306 is preferably sufficiently small so that random defects are unlikely to occur in the same cell location 306 and so that finding a physical feature of the die within one of the cell locations 306 may be performed in a reasonable amount of time. For example, the size of each of the cell locations 306 may be selected so that the probability of more than one random defect occurring in the same cell location 306 is than a selected threshold, for example, .01. However, the size of each of the cell locations 306 should also be large

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enough so that several tested nets are likely to pass through, that is, intersect the same cell location 306. For typical integrated circuit manufacturing processes, a grid spacing 302 of about 50 to 200 microns is generally sufficient to meet these criteria."

Absent a logical basis and technical reasoning for selecting the claimed grid spacing of 50 to 200 microns over any other grid spacing that provides sufficient channel for routing test paths in Vo, the claimed grid spacing of 50 to 200 microns is not obvious under 35 U.S.C. § 103(a).

Applicant respectfully requests examination and favorable reconsideration of Claims 1-20.

No additional fee is believed due for this amendment.

Respectfully submitted,


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